What is Claimed is:

1. A semiconductor device having a chip-on-chip structure wherein a first semiconductor chip having a circuit block where a plurality of inter-chip connection terminals and a plurality of external connection terminals are formed on a surface of the chip and a second semiconductor chip having a circuit block where a plurality of inter-chip connection terminals and a plurality of external connection terminals are formed on a surface of the chip are adhered to each other in a form wherein the surfaces of the chips are opposed to each other so that the inter-chip connection terminals of said first semiconductor chip and the inter-chip connection terminals of said second semiconductor chip are connected to each other, wherein

said first semiconductor chip comprises a first multiplexer circuit for selecting an input signal line from among a plurality of input signal lines so as to output a signal from the selected input signal line to an output signal line, and the output signal line of said first multiplexer circuit is connected to an inter-chip connection terminal of said first semiconductor chip.

2. The semiconductor device according to Claim 1, wherein at least one input signal line from among the plurality of input signal lines inputted to said first

multiplexer circuit is connected to an external connection terminal of said first semiconductor chip.

3. The semiconductor device according to Claim 2, wherein said first semiconductor chip comprises a first operation mode setting circuit and wherein said first multiplexer circuit is controlled by an operation mode setting signal outputted from said first operation mode setting circuit.

4. The semiconductor device according to Claim 1, wherein said first semiconductor chip comprises a first demultiplexer circuit for selecting any one of a plurality of output signal lines, and for outputting a signal from an input signal line to the selected output signal line, and wherein the input signal line inputted to said first demultiplexer circuit is connected to an inter-chip connection terminal of said first semiconductor chip.

5. The semiconductor device according to Claim 4, wherein at least one output signal line from among the plurality of output signal lines outputted from said first demultiplexer circuit is connected to an external connection terminal of said first semiconductor chip.

6. The semiconductor device according to Claim 5, wherein said first semiconductor chip comprises a first operation mode setting circuit and wherein said first demultiplexer circuit is controlled by an operation mode

setting signal outputted from said first operation mode setting circuit.

7. The semiconductor device according to Claim 1, wherein said first semiconductor chip comprises a second demultiplexer circuit for selecting any one of a plurality of output signal lines, and for outputting a signal from an input signal line to the selected output signal line, and wherein at least one output signal line from among the plurality of output signal lines outputted from said second demultiplexer circuit is connected to an external connection terminal of said first semiconductor chip.

8. The semiconductor device according to Claim 7, wherein at least one output signal line from among the plurality of output signal lines outputted from said second demultiplexer circuit is connected to one of the plurality of input signal lines inputted to said first multiplexer circuit.

9. The semiconductor device according to Claim 8, wherein said first semiconductor chip comprises a first operation mode setting circuit, and wherein said second demultiplexer circuit is controlled by an operation mode setting signal outputted from said first operation mode setting circuit.

10. The semiconductor device according to Claim 4, wherein said first semiconductor chip comprises a second

multiplexer circuit for selecting an input signal line from among a plurality of input signal lines and for outputting a signal from the selected input signal line to an output signal line, and wherein at least one input signal line from among the plurality of input signal lines inputted to said second multiplexer circuit is connected to an external connection terminal of said first semiconductor chip.

11. The semiconductor device according to Claim 10, wherein at least one input signal line from among the plurality of input signal lines inputted to said second multiplexer circuit is connected to one of the plurality of output signal lines outputted from said first demultiplexer circuit.

12. The semiconductor device according to Claim 11, wherein said first semiconductor chip comprises a first operation mode setting circuit, and wherein said second multiplexer circuit is controlled by an operation mode setting signal outputted from said first operation mode setting circuit.

13. The semiconductor device according to Claim 1, wherein said second semiconductor chip comprises a third demultiplexer circuit for selecting any one of a plurality of output signal lines, and for outputting a signal from an input signal line to the selected output signal line, and wherein the input signal line inputted to said third

demultiplexer circuit is connected to an inter-chip connection terminal of said second semiconductor chip.

14. The semiconductor device according to Claim 13, wherein said second semiconductor chip comprises a second operation mode setting circuit, and wherein said third demultiplexer circuit is controlled by an operation mode setting signal outputted from said second operation mode setting circuit.

15. The semiconductor device according to Claim 13, wherein said second semiconductor chip comprises a third multiplexer circuit for selecting an input signal line from among a plurality of input signal lines and for outputting a signal from the selected input signal line to an output signal line, and wherein the output signal line of said third multiplexer circuit is connected to an inter-chip connection terminal of said second semiconductor chip.

16. The semiconductor device according to Claim 15, wherein said second semiconductor chip comprises a second operation mode setting circuit, and wherein said third multiplexer circuit is controlled by an operation mode setting signal outputted from said second operation mode setting circuit.

17. The semiconductor device according to Claim 13, wherein said second semiconductor chip comprises a fourth multiplexer circuit for selecting an input signal line from

among a plurality of input signal lines and for outputting a signal from the selected input signal line to an output signal line, and wherein at least one input signal line from among the plurality of input signal lines inputted to said fourth multiplexer circuit is connected to an external connection terminal of said second semiconductor chip.

18. The semiconductor device according to Claim 17, wherein at least one input signal line from among the plurality of input signal lines inputted to said fourth multiplexer circuit is connected to one of the plurality of output signals outputted from said third demultiplexer circuit.

19. The semiconductor device according to Claim 18, wherein said second semiconductor chip comprises a second operation mode setting circuit, and wherein said fourth multiplexer circuit is controlled by an operation mode setting signal outputted from said second operation mode setting circuit.

20. The semiconductor device according to Claim 15, wherein said second semiconductor chip comprises a fourth demultiplexer circuit for selecting any one of a plurality of output signal lines, and for outputting a signal from an input signal line to the selected output signal line, and wherein at least one output signal line from among the plurality of output signal lines outputted from said fourth

demultiplexer circuit is connected to an external connection terminal of said second semiconductor chip.

21. The semiconductor device according to Claim 20, wherein at least one output signal line from among the plurality of output signal lines outputted from said fourth demultiplexer circuit is connected to one of the plurality of input signal lines inputted to said third multiplexer circuit.

22. The semiconductor device according to Claim 21, wherein said second semiconductor chip comprises a second operation mode setting circuit, and wherein said fourth demultiplexer circuit is controlled by an operation mode setting signal outputted from said second operation mode setting circuit.

23. A semiconductor device having a chip-on-chip structure wherein; a first semiconductor chip, incorporating a first circuit block, where first and second inter-chip connection terminals and first and second external connection terminals are formed on a surface of the chip; and a second semiconductor chip, incorporating a second circuit block provided with input and output terminals for a normal operation mode and input and output terminals for a test mode, so that a signal is transmitted to, and is received from, said first circuit block via input and output terminals for said normal operation mode,

where third and fourth inter-chip connection terminals and third and fourth external connection terminals are formed on a surface of the chip; are adhered to each other in a form wherein the surfaces of the chips are opposed to each other, and wherein said first and third inter-chip connection terminals are connected to each other, and said second and fourth inter-chip connection terminals are connected to each other; wherein

said first semiconductor chip comprises:

a first signal channel setting switching circuit for setting signal channels between an output terminal of said first circuit block as well as said first external connection terminal, and said first inter-chip connection terminal; and

a second signal channel setting switching circuit for setting signal channels between said second inter-chip connection terminal and an input terminal of said first circuit block as well as said second external connection terminal, wherein

a first operation mode setting signal is inputted to said first and second signal channel setting switching circuits and said first signal channel setting switching circuit sets a signal channel for connecting the output terminal of said first circuit block to said first inter-chip connection terminal and said second signal channel

setting switching circuit sets a signal channel for connecting said second inter-chip connection terminal to the input terminal of said first circuit block when said first operation mode setting signal indicates the normal operation mode, and

said first signal channel setting switching circuit sets a signal channel for connecting said first external connection terminal to said first inter-chip connection terminal and said second signal channel setting switching circuit sets a signal channel for connecting said second external connection terminal to said second inter-chip connection terminal when said first operation mode setting signal indicates a first test mode of said second circuit block, and wherein

said second semiconductor chip comprises:

a third signal channel setting switching circuit for setting signal channels between said third inter-chip connection terminal as well as said third external connection terminal, and the input terminal for the normal operation mode as well as the input terminal for the test mode of said second circuit block; and

a fourth signal channel setting switching circuit for setting signal channels between the output terminal for the normal operation mode as well as the output terminal for the test mode of said second circuit block and said

fourth inter-chip connection terminal as well as said fourth external connection terminal, wherein

a second operation mode setting signal is inputted to said third and fourth signal channel setting switching circuit and said third signal channel setting switching circuit sets a signal channel for connecting said third inter-chip connection terminal to the input terminal for the normal operation mode of said second circuit block and said fourth signal channel setting switching circuit sets a signal channel for connecting the output terminal for the normal operation mode of said second circuit block to said fourth inter-chip connection terminal when said second operation mode setting signal indicates the normal operation mode,

said third signal channel setting switching circuit sets a signal channel for connecting said third inter-chip connection terminal to the input terminal for the test mode of said second circuit block and said fourth signal channel setting switching circuit sets a signal channel for connecting the output terminal for the test mode of said second circuit block to said fourth inter-chip connection terminal when said second operation mode setting signal indicates said first test mode of said second circuit block, and

said third signal channel setting switching circuit sets a signal channel for connecting said third external connection terminal to the input terminal for the test mode of said second circuit block and said fourth signal channel setting switching circuit sets a signal channel for connecting the output terminal for the test mode of said second circuit block to said fourth external connection terminal when said second operation mode setting signal indicates the second test mode of said second circuit block.

24. The semiconductor device according to Claim 23, wherein said first semiconductor chip comprises:

a fifth external connection terminal connected to said first signal channel setting switching circuit; and a sixth external connection terminal connected to said second signal channel setting switching circuit, wherein

said first signal channel setting switching circuit sets a signal channel for connecting the output terminal of said first circuit block to said fifth external connection terminal and said second signal channel setting switching circuit sets a signal channel for connecting said sixth external connection terminal to the input terminal of said first circuit block when said first operation mode setting signal indicates the test mode of said first circuit block.

25. The semiconductor device according to Claim 23, wherein said first semiconductor chip comprises a first

operation mode setting circuit for outputting said first operation mode setting signal to said first and second signal channel setting switching circuits, and wherein said second semiconductor chip comprises a second operation mode setting circuit for outputting said second operation mode setting signal to said third and fourth signal channel setting switching circuits.

26. The semiconductor device according to Claim 24, wherein said first semiconductor chip comprises a first operation mode setting circuit for outputting said first operation mode setting signal to said first and second signal channel setting switching circuits, and wherein said second semiconductor chip comprises a second operation mode setting circuit for outputting said second operation mode setting signal to said third and fourth signal channel setting switching circuits.

27. A semiconductor device having a chip-on-chip structure wherein; a first semiconductor chip, incorporating a first circuit block, where first and second inter-chip connection terminals and first and second external connection terminals are formed on a surface of the chip; and a second semiconductor chip, incorporating a second circuit block provided with input and output terminals for a normal operation mode and input and output terminals for a test mode, so that a signal is transmitted

to, and is received from, said first circuit block via input and output terminals for said normal operation mode, where third and fourth inter-chip connection terminals and third and fourth external connection terminals are formed on a surface of the chip; are adhered to each other in a form wherein the surfaces of the chips are opposed to each other, and wherein said first and third inter-chip connection terminals are connected to each other, and said second and fourth inter-chip connection terminals are connected to each other; wherein

said first semiconductor chip comprises:

a first multiplexer circuit to which signals from an output terminal of said first circuit block and from said first external connection terminal are inputted and which selects either one of the signals inputted to the first multiplexer circuit based on a first operation mode setting signal so that the selected signal is outputted to said first inter-chip connection terminal; and

a first demultiplexer circuit to which a signal from said second inter-chip connection terminal is inputted, and which selects either the input terminal of said first circuit block or said second external connection terminal based on said first operation mode setting signal, and which outputs a signal inputted from said second inter-chip connection terminal to the selected terminal, wherein

said first multiplexer circuit selects a signal from the output terminal of said first circuit block and said first demultiplexer circuit selects an input terminal of said first circuit block when said first operation mode setting signal indicates the normal operation mode, and

said first multiplexer circuit selects a signal from said first external connection terminal and said first demultiplexer circuit selects said second external connection terminal when said first operation mode setting signal indicates a first test mode of said second circuit block, and wherein

said second semiconductor chip comprises:

a second demultiplexer circuit to which a signal is inputted from said third inter-chip connection terminal, and which has an output terminal connected to the input terminal for the normal operation mode of said second circuit block and an output terminal that is connectable to the input terminal for the test mode of said second circuit block and which selects either one of the two output terminals of the second demultiplexer circuit based on a second operation mode setting signal and which outputs a signal inputted from said third inter-chip connection terminal to the selected output terminal;

a second multiplexer circuit to which signals are inputted from the output terminal of said second

demultiplexer circuit that is connectable to the input terminal for the test mode of said second circuit and from said third external connection terminal, and which selects either one of the signals inputted to the second multiplexer circuit based on a third operation mode setting signal and which outputs the selected signal to the input terminal for the test mode of said second circuit block;

a third multiplexer circuit, having an input terminal connected to the output terminal for the normal operation mode of said second circuit block and an input terminal that is connectable to the output terminal for the test mode of said second circuit block, which selects either one of the two input terminals of the third multiplexer circuit based on said second operation mode setting signal and which outputs a signal inputted to the selected input terminal to said fourth inter-chip connection terminal; and

a third demultiplexer circuit to which a signal is inputted from the output terminal for the test mode of said second circuit block, and which selects either the input terminal of said third multiplexer circuit that is connectable to the output terminal for the test mode of said second circuit block or said fourth external connection terminal based on said third operation mode setting signal and which outputs a signal inputted from the

output terminal for the test mode of said second circuit block to the selected terminal, wherein

said second demultiplexer circuit selects the output terminal connected to the input terminal for the normal operation mode of said second circuit block, and said third multiplexer circuit selects the input terminal connected to the output terminal for the normal operation mode of said second circuit block, when said second operation mode setting signal indicates the normal operation mode,

said second demultiplexer circuit selects the output terminal that is connectable to the input terminal for the test mode of said second circuit block, and said third multiplexer circuit selects the input terminal that is connectable to the output terminal for the test mode of said second circuit block, when said second operation mode setting signal indicates said first test mode of said second circuit block,

said second multiplexer circuit selects a signal from an output terminal of said second demultiplexer circuit, and said third demultiplexer circuit selects an input terminal of said third multiplexer circuit, when said third operation mode setting signal indicates said first test mode of said second circuit block, and

said second multiplexer circuit selects a signal from said third external connection terminal, and said

third demultiplexer circuit selects said fourth external connection terminal, when said third operation mode setting signal indicates a second test mode of said second circuit block.

28. The semiconductor device according to Claim 27, wherein said first semiconductor chip comprises:

fifth and sixth external connection terminals;

a fourth demultiplexer circuit, inserted between the output terminal of said first circuit block and said first multiplexer circuit, to which an output signal of said first circuit block is inputted and which selects either said first multiplexer circuit or said fifth external connection terminal based on a fourth operation mode setting signal and which outputs an output signal from said first circuit block, that is inputted, to the selected circuit or the selected terminal; and

a fourth multiplexer circuit, inserted between the input terminal of said first circuit block and said first demultiplexer circuit, to which an output signal from said first demultiplexer circuit and a signal from said sixth external connection terminal are inputted, and which selects either of the signals inputted to the fourth multiplexer circuit based on said fourth operation mode setting signal and which outputs the selected signal to said first circuit block, wherein

said fourth demultiplexer circuit selects said first multiplexer circuit, and fourth multiplexer circuit selects an output signal from said first demultiplexer circuit, when said fourth operation mode setting signal indicates the normal operation mode, and

said fourth demultiplexer circuit selects said fifth external connection terminal, and said fourth multiplexer circuit selects a signal from said sixth external connection terminal, when said fourth operation mode setting signal indicates the test mode of said first circuit block.

29. The semiconductor device according to Claim 27, wherein said first semiconductor chip comprises a first operation mode setting circuit for outputting said first operation mode setting signal to said first multiplexer circuit and to said first demultiplexer circuit; and said second semiconductor chip comprises a second operation mode setting circuit for outputting said second operation mode setting signal to said second demultiplexer circuit and to said third multiplexer circuit and for outputting said third operation mode setting signal to said second multiplexer circuit and to said third demultiplexer circuit.

30. The semiconductor device according to Claim 28, wherein said first semiconductor chip comprises a first operation mode setting circuit for outputting said first

operation mode setting signal to said first multiplexer circuit and to said first demultiplexer circuit and for outputting said fourth operation mode setting signal to said fourth demultiplexer circuit and to said fourth multiplexer circuit; and said second semiconductor chip comprises a second operation mode setting circuit for outputting said second operation mode setting signal to said second demultiplexer circuit and to said third multiplexer circuit and for outputting said third operation mode setting signal to said second multiplexer circuit and to said third demultiplexer circuit.